Docket No.: 1514.1032

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Ji Yong PARK et al.

Application No. 10/690,507 Group Art Unit: 1792

Confirmation No. 6043

Filed: October 23, 2003 Examiner: Matthew J. Song

For: METHOD FOR MANUFACTURING POLYCRYSTALLINE SILICON THIN FILM AND THIN FILM TRANSISTOR FABRICATED USING POLYCRYSTALLINE SILICON THIN FILM MANUFACTURED BY THE MANUFACTURING METHOD

SUBMISSION OF COLOR COPIES OF DECLARATION UNDER RULE 132 AND EXHIBIT A

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Supplemental to Applicants' earlier submission in support of RCE electronically filed on March 26, 2008; enclosed are copies of 1) Declaration Under Rule 132 and 2) Exhibit A "Design of SLS crystallization method for Low Temperature Poly-Si TFT" by Inventor Hye-Hang Park (both in color) only the Examiner's convenience. Consideration is respectfully requested.

Respectfully submitted,

STEIN, MCEWEN & BUI LLP

Date: 3/28/08 By: _____
Hung H. Bui
Registration No. 40,415

1400 Eye St. N.W., Suite 300
Washington, D.C. 20005
Telephone: (202) 216-9505
Facsimile: (202) 216-9510

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Hye Hyang PARK et al.

Application No. 10/690,507 Group Art Unit: 1792

Confirmation No. 6043

Filed: October 23, 2003 Examiner: Matthew J. Song

For: METHOD FOR MANUFACTURING POLYCRYSTALLINE SILICON THIN FILM AND THIN FILM TRANSISTOR FABRICATED USING POLYCRYSTALLINE SILICON THIN FILM MANUFACTURED BY THE MANUFACTURING METHOD

Declaration Under Rule 132

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sirs:

I, Hye-Hyang Park, have received a degree in Master from Seoul National Univ. and have 8 years of experience in the field of thin film transistors and am aware of the state of the art from the time of 2001 to the present.

I am a researcher employed by Samsung SDI Co., LTD, and have worked on designing SLS crystallization methods with the Technology Development Team 1 at the Corporate R & D Center of Samsung SDI Co., LTD, currently located at 428-5, Gongse-Ri, Kiheung-Eup, Yongin-City, Gyeonggi-Do, 449-902, South Korea.

I am a co-inventor of the invention disclosed in the above-referenced patent application (U.S. Patent Application No. 10/690,507), and am responsible for writing the article entitled "Design of SLS crystallization method for Low Temperature Poly-Si TFT," a copy of which is enclosed in Exhibit A, and which discusses the scientific basis for the invention disclosed in the above-referenced patent application.

I have reviewed and understand the prior art references, including Jung, U.S. Patent No. 6,825,493, and Yang, U.S. Publication No. 2002/019775, all the claims as pending in the instant application, and the arguments in the Office Action, and am familiar with thin film transistor (TFT) technology.

BACKGROUND INFORMATION

Sequential lateral solidification (SLS) crystallization technology is a promising lateral growth technique used to form large silicon grains from polycrystalline or single crystalline grains. The large silicon grains formed by SLS crystallization technology can then be used to make thin film transistors (TFTs) with superior performance for fabrication of highly circuit-integrated flat panel displays, such as TFT LCD (Liquid Crystal Display) and TFT OLED (Organic Light Emitting Display). To crystallize silicon using the SLS crystallization technology, a laser beam is irradiated onto an amorphous silicon layer two or more times, so that the laser beam is overlappingly irradiated on the layer, thereby growing the side of crystalline silicon. However, there are at least two problems with this conventional method for crystallizing silicon:

1. Fatal grain boundaries are likely included in the active channel regions, since this conventional method uses grains having a limited size. The performance of poly-Si TFTs is extremely dependent on grain boundaries, and the field effect mobility of TFTs having a channel direction from source to drain which is perpendicular to the lateral grain growth direction is remarkably smaller than the field effect mobility of TFTs having parallel channel growth direction.

2. TFT characteristics vary according to a gap (width of grains) between grains having the same length and growing direction that are arranged side to side, even in the case that the direction of the active channels is parallel to the growing direction. As a result, when the width of the grains is small, the mobility of an electric field is greatly deteriorated by a scattering effect during charge transfer.

DEVELOPMENT OF SOLUTION TO THE CONVENTIONAL PROBLEMS

Recognizing these conventional problems with SLS crystallization technology, I helped develop an improved SLS crystallization method in early 2002-2003, which is disclosed and claimed in the above-referenced patent application. Independent claims 1, 6, and 13 generally define a method of manufacturing polycrystalline silicon thin film, and claim 1 specifically defines forming an amorphous silicon layer on a substrate, and irradiating the amorphous silicon layer using a laser beam, and transversely moving the mask relative to the substrate by a distance such that the laser beam is overlappingly irradiated at an overlapping region on the substrate where amorphous silicon and a par of already crystallized polycrystalline silicon are exposed so as to increase an average width of the polycrystalline silicon grains, wherein a width of the overlapping region during crystallization corresponds to the distance, and is varied from no less than 0.5 μm to 2.0μm, and wherein the average width of the polycrystalline silicon grains is varied between approximately 0.2μm and 0.6μm, and is decreased when the width of the overlapping region on which the laser beam is overlappingly irradiated is decreased.

As a result of the claimed method, TFTs can be manufactured which have average grain widths of 0.2 μm to 0.6μm, that are small but result in TFTs with superior electric field mobility characteristics. Specifically, as described at pages 4-5 of Exhibit A, by increasing the overlap from 0.5μm to 2.0μm, we increased the grain width about three times, from approximately 0.2μm to 0.6μm. Significantly, we also observed, as explained at page 5 of Exhibit A, that as

the overlap increased from 0.5μm to 2.0μm, both field effect mobility and threshold voltage tended to be nearly constant with little variation (as shown in FIG. 7 of Exhibit A), which is a result that is somewhat contrary to other results in conventional scientific literature.

UNEXPECTED RESULTS

In my opinion, the method claimed by the instant application produces unexpected results which support the non-obvious nature of the invention. As shown in FIG. 4 of Exhibit A, as the overlap between the 1st and 2nd laser pulses increases from 0.5μm to 2.0μm, the average grain width of the grains increases from approximately 0.2μm to 0.6μm:

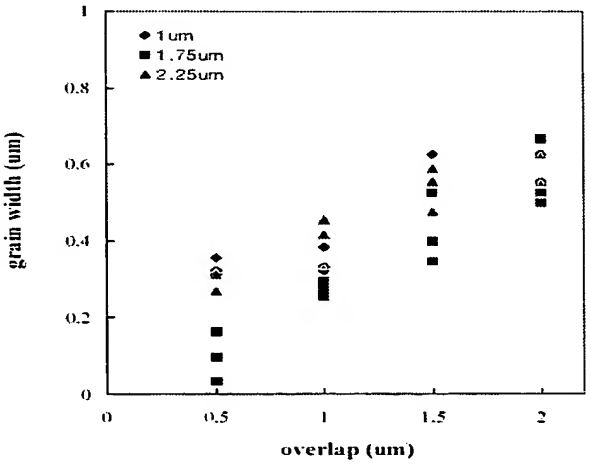


Fig. 4. Dependence of average grain width on the overlap between the 1st and the 2nd laser pulses. The grain width was measured at positions of 1μm, 1.75μm, and 2.25μm away from the primary grain boundary.

Furthermore, as shown in FIG. 7 of Exhibit A (alternatively, FIG. 3 of the instant application), when the overlap was 0.5μm, the field effect mobility was relatively low, ranging from 225 cm^2/Vs to 302 cm^2/Vs; however, as the overlap increased from 0.5μm to 2.0μm, both field effect mobility and threshold voltage tended to be nearly constant with smaller variation:

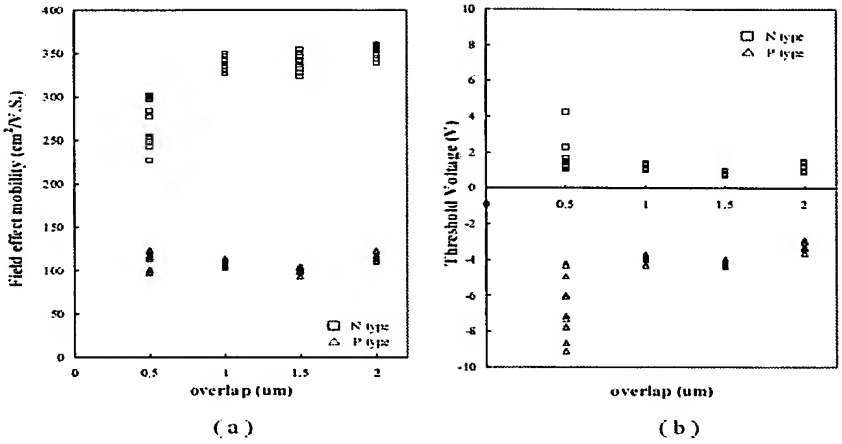


Fig. 7. Dependence of (a) field effect mobility and (b) threshold voltage on the overlap between the 1st and the 2nd laser pulses.

As stated at page 5 of Exhibit A:

> "This result [the nearly constant field effect mobility and threshold voltage as the overlap increases from 0.5μm to 2.0μm] is somewhat contrary to other results in the literature, which reported that for thin poly-si films, as poly-Si grain width decreased, TFT field effect mobility tended to decrease. As a result, when the poly-Si grain width is larger than about 0.2μm, the n-channel TFT field effect mobility is only slightly affected by the poly-Si grain width, however, the mobility is significantly decreased for the thinner film (see FIG. 8 of Exhibit A)."

We postulated that the reason for this unexpectedly slight variation in field effect mobility and threshold voltage is "possibly because thin poly-Si film has high thermal stress during crystallization due to a fast cooling rate compared to thick film, resulting in an increase of intra-grain defects such as twin and sub-boundary, so that the film thickness may significantly affect TFT properties." Thus, we discovered that the width of the grains is highly significant because the grains exhibit the unexpected property of having only slight variations in field effect mobility and threshold voltage once the grain width exceeds 0.2μm but not greater than 0.6μm, which is contrary to the results predicted by other scientific literature in the field.

Practically speaking, as a result of this unexpectedly slight variation in field effect mobility and threshold voltage based on the claimed grain widths, we proposed designing mask patterns which have an overlap which is not less than 1μm. By using these improved mask patterns, we can develop TFTs which have superior properties and improved field effect mobility. These superior TFTs can then be used to develop other technologies, such as an advanced ideal display called a SOP (System On Panel).

PRIOR ART REFERENCES

I have not found that prior art references disclosed, for example, in Jung, U.S. Patent No. 6,825,493 (hereinafter, "Jung '493"), and Yang, U.S. Patent Application Publication No. 2002/0197759 (hereinafter, "Yang '759") correspond to claims(s) 1-3, 6-8, 10 and 13-14 for the following reasons:

1. Jung '493 discloses a conventional sequential lateral solidification (SLC) crystallization method in which a single mask is used to fabricate both switching circuits, such as, TFTs, and driving circuits, such as, CMOS devices, in order to reduce the process time and to improve production. Such a mask 130 is shown in FIG. 5, including light transmitting portions 132 and light absorptive portions 134. Each light transmitting portion 132 has a width of 2 micrometers (μm). Each light absorptive portion 134 has a width of 10 micrometers (μm). Such a mask 130 is used differently depending upon whether the crystallization process is utilized for the driving circuits, i.e., CMOS devices, as shown in FIGs. 6A-6D, or alternatively, for the switching circuits, i.e., TFTs, as shown in FIGs. 7A-7D. For example, in the embodiment shown in FIGs. 6A-6D, the mask 130 is used to move along the lateral grain growth of the grains (see FIG. 6A) in a X-direction by a distance of about 0.7 micrometers (see column 9, lines 54-55 of Jung '493) during the fabrication of the driving circuits, i.e., CMOS devices. As a result, the polycrystalline silicon grains are obtained with a width "P" of 12 micrometers (see column 10, lines 8-10 of Jung '493). In a separate embodiment shown in FIGs. 7A-7D, the mask 130 is used to move in a X-direction by a distance of about 1.7 micrometers (see column 10, lines 40-41 of Jung '493) during the fabrication of the switching circuits, i.e., TFTs. As a result, the resulting grains are obtained with a width of 1.7 micrometers (see column 10, lines 64-65 of Jung '493). According to Jung '493, each grain has a width of about 1.7 micrometers (μm) (see column 10, lines 64-65 of Jung '493), which is sufficient for the active layers of the TFTs (see column 11, lines 2-5 of Jung '493).

2. According to Jung '493, the smallest width for the polycrystalline silicon grains can be obtained is 1.7 micrometers (μm), which is entirely consistent with what was disclosed in the Background of the instant application. In other words, if the width of the polycrystalline silicon grains is made smaller than the conventional width of 1.7 micrometers (μm) as disclosed in Jung '493, then the mobility of an electric field is greatly deteriorated by a scattering effect during charge transfer; see paragraph [0009] of Applicants' disclosure.

3. Jung '493 does not disclose each of the recited features of a "width of the overlapping region during crystallization corresponds to the distance, and is varied from no less than 0.5 μm to 2 μm," and "the average width of the polycrystalline silicon grains is varied between

approximately 0.2 μm and 0.6 μm, and is decreased when the width of the overlapping region on which the laser beam is overlappingly irradiated is decreased," as recited by Applicants' independent claims 1 and 13.

4. More importantly, the grains illustrated in FIG. 3C of Jung '493 are not illustrated or described as having an average width which is "varied between approximately 0.2 μm and 0.6 μm," as recited by Applicants' independent claims 1 and 13. Moreover, FIG. 3C of Jung '493 does not show silicon grains having a width approximately within the claimed range based on the 0.7 micrometer scale. Rather, as described on column 3, lines 49-61 of Jung '493, FIG. 3C is an enlarged view of how a mask translates across the sample substrate by a distance of 0.7 micrometers in a transverse direction (i.e., in the x-axial direction). According to Jung '493, when the same mask moves by 0.7 micrometers, the average width of the grains becomes 12 micrometers (see column 10, lines 8-10 of Jung '493) in the driving circuit (CMOS) area, and 1.7 micrometers (see column 10, lines 64-65 of Jung '493) in the switching circuit (TFT) area.

5. Yang '759 does not show at least the recited feature of "wherein the laser transmission region is wider than the laser non-transmission region by more than 1 μm," as defined in claim 6. As described in paragraph [0067] of Yang '759, the light transmission regions L and M have tier-shaped top and bottom outlines. Each of first light transmission regions L is comprised of first to fourth rectangular-shaped patterns, all having the same width. Yang '759 does not teach or suggest a "laser transmission region" which is "wider than the laser non-transmission region by more than 1 μm," as defined in claim 6.

CONCLUSION

In conclusion, it is my belief and understanding that the method disclosed in the above-referenced patent application exhibits unexpected results for the claimed range of an average grain width which is "varied between approximately 0.2 μm and 0.6 μm." The conventional literature predicted that for thin poly-si films, as the poly-Si grain width decreased, TFT field effect mobility tended to decrease. However, as described in the enclosed article, we discovered that by varying the average grain width between approximately 0.2 μm and 0.6 μm, the grains exhibited the unexpected result that when the poly-Si grain width is larger than about 0.2μm, the n-channel TFT field effect mobility is only slightly affected by the poly-Si grain width.

The Declarant further states that the above statements were made with the knowledge that willful false statements and the like are punishable by fine and/or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that any such willful false statement may jeopardize the validity of this application or any patent resulting therefrom.

By: Hye Hyang Park Date March 25, 2008

Hye Hyang PARK

On this 25 day of March 2008, before me personally appeared Hye-Hyang PARK, to me known and known to me to be the individual described in and who executed the foregoing instrument, and who thereupon acknowledged to me that he executed the same for the purposes set forth therein.

_____

EXHIBIT A

Title: Design of SLS crystallization method for Low Temperature Poly-Si TFT
Inventor: Hye-Hang Park

Design of SLS crystallization method for Low Temperature Poly-Si TFT

Ji-Yong Park, Hye-Hyang Park, Ki–Yong Lee, and Ho-Kyoon Chung

Technology Development Team 1, Corporate R&D Center, Samsung SDI Co., LTD

428-5, Gongse-Ri, Kiheung-Eup, Yongin-City, Gyeonggi-Do, 449-902, KOREA

Sequential lateral solidification (SLS) is known to be a promising method to make low temperature poly-Si thin film transistors (LTPS TFT) with superior performance for fabrication of highly circuit-integrated flat panel displays such as TFT LCD (Liquid Crystal Display) and TFT OLED (Organic Light Emitting Diode). In this work we studied the dependence of TFT characteristics on SLS poly-Si grain width and suggested the methods of designing SLS mask pattern to achieve uniform TFT performance. We varied the width of poly-Si grain by employing the 2-shot SLS mask pattern with different overlap between 1st and 2nd laser pulses. The width of poly-Si grain decreased with decreasing the overlap. However, the measured TFT characteristics revealed that the width of poly-Si grain little influences on the device properties. We could achieve the TFT mobility about 350cm^2/V.sec for the overlap not less than 1μm. We suggested that SLS mask pattern (x, y) should be designed that $2+y \leq x < 2$(***C-SLG distance***) and $y >$ (***optical resolution***), where x is the spacing of the laser absorbed region and y is the spacing of the laser non-absorbed region on the substrate.

Keyword : TFT, crystallization, poly-Si, grain, mask pattern

I . INTRODUCTION

The high mobility of low temperature poly-Si TFT enables external ICs to drive the pixels to be integrated on a panel. This yields a light and thin display with reduction of connection pins and also improves both the reliability of the panel and the resolution of displays. Further improvement of poly-Si TFT's performances enables the memory and controller to be integrated on a glass panel and an advanced ideal display so called SOP (System On Panel) can be realized [1,2].

Poly-Si TFTs based on conventional ELA (Eximer Laser Annealing) method allows a limited integration of circuits because of the relatively low field effect mobility of 50~200cm^2/V.sec. For the ELA crystallization, non-uniformity of grain size and narrow process window make it difficult to achieve uniform TFT performance[1,3]. Therefore, the key technology to achieve the SOP (System On Panel) is to improve both the performance and uniformity of TFTs. To satisfy these needs, several crystallization method based on lateral growth technique such as SELAX (Selectively Enlarging Laser X'tallization)[4], DPSS (Diode Pumped Solid State) CLC (CW Laser Lateral Crystallization)[5-7] and SLS (Sequential Lateral Solidification)[8-10] technology have been proposed. Among these technologies, SLS process utilizes Controlled Super Lateral Growth (C-SLG) that relies on inducing complete melting of selected region of the Si film via irradiation through a patterned mask. Using repeated C-SLG inducing laser irradiation through specially designed mask pattern and precise translation of the film with respect to the pre-molten region, SLS process makes it possible to realization of various microstructures that lead to various device performances[11].

The mobility of TFTs integrated on poly-Si film crystallized by SELAX[4], CLC[6], and SLS[9-14] was reported to be more than 300cm^2/V.sec. The performance of poly-Si TFTs is known to be extremely dependent on the grain boundary[11,15,16]. Field effect mobility of TFTs whose channel direction from source to drain is perpendicular to the lateral grain growth direction, was remarkably lower than the mobility of TFTs having parallel channel direction. This is because relatively more grain boundaries are included in the channel region of TFT for the perpendicular channel direction compared to the parallel one[7,11-14]. Thus, many researchers have focused on enlarging the length of laterally grown poly-Si grain to decrease the number of grain boundaries in the channel region of TFT, which play a role as barriers for the current flow[6-14]. In addition to the effect of the length of poly-Si grain, it is also reported that the field effect mobility depends on the width of poly-Si grain[4,14,17]. The field effect mobility was increased with increasing the width of poly-Si grain. Hatano et al [4,14,17] reported that the width of poly-Si grain varied depending on the process parameters such as film thickness and laser fluence.

The purpose of the present work is to study the effects of poly-Si grain width on the TFT performance. In particular, we employed the 2-shot SLS mask pattern to vary the overlap between 1st laser pulse and 2nd laser pulse without changing other process parameters such as film thickness, pulse duration etc. Based on the experimental results obtained in this study, we attempt to suggest the methods of designing the SLS mask pattern to achieve uniform poly-Si TFT characteristics.

Ⅱ. EXPERIMENTALS

Top gate coplanar structured TFTs were fabricated on the Corning 1737 glass substrate by low temperature processes. Buffer SiO_2 films and 800 Å-thick amorphous silicon films were deposited on the glass substrate by PECVD and subsequently the films were de-hydrogenated by furnace annealing. After dehydrogenation, the a-Si films were crystallized using SLS process. A 308nm XeCl excimer laser beam whose pulse duration was extended 5 times was used for irradiation. The laser beam was spatially homogenized and subsequently shaped using a mask made of a Cr-coated quartz plate. The shaped laser beam was imaged on the film through the projection lens with 5× demagnifications.

For the SLS process, 2-shot SLS method was used for this study (Figure 1). When x is the spacing of the laser absorbed region and y is the spacing of the laser non-absorbed region on the substrate, the mask pattern consists of a number of laser-transparent slits of $5x$ μm spacing and laser non-transparent Cr coated region of $5y$ μm spacing (Figure 1a). We define the dimension of the mask pattern as (x, y) on the basis of 5× demagnified values on the substrate. The pulsed laser beam is irradiated at an energy density sufficient to induce complete melting of a-Si. The laser beam irradiated through the transparent region of the mask pattern is strongly absorbed within a few atomic layers of Si film surface, melting the film completely, while the laser beam irradiated on the non-transparent region is reflected from the mask, leaving the Si film as solid phase. Subsequently the molten Si begins to cool and the poly-Si grain grows laterally from un-molten region (edge of the transparent pattern) to fully molten region (center of the transparent pattern) [18-22]. Then the actual crystallized poly-Si region on the substrate is about xμm, while the actual non-crystallized a-Si region on the substrate is about y μm in spacing due to 5× demagnifications through the projection lens. When two opposite growth fronts collide with each other, a 'primary grain boundary', which has high grain boundary protrusion, forms in the middle of the transparent region (Figure 1b). After translating the mask pattern in a direction parallel to the primary grain boundary, the 2nd laser pulse is irradiated to enlarge the poly-Si grains which were formed by the 1st laser pulse. By the 2nd laser pulse, a portion of the poly-Si region formed by the 1st laser pulse (***overlap*** = $(x-y)/2$, in Figure 1c) remelts, and thus the molten zone formed by the second laser pulse becomes to contact with the previous laterally grown poly-Si grains crystallized by the 1st laser beam. Then the poly-Si grains continuously grow into the molten zone increasing the grain length. The solid circle in Figure 1d indicates the resulting poly-Si grains enlarged laterally by 2 sequential laser shots. Therefore for the 2-shot SLS processed poly-Si, the width of poly-Si grains can be defined as the spacing between two adjacent laterally grown grains (Figure 1d). Likewise we can define the length of poly-Si grains as the spacing between two adjacent primary grain boundaries (Figure 1d). Then the length of the final poly-Si grains formed by the 2-shot SLS can be simply calculated to be $(x+y)/2$, which is determined by a mask pattern.

To study the effects of grain width on the TFT performance, we varied the width by employing various SLS crystallization mask pattern dimensions. With a fixed grain length of $(x+y)/2$=3.5μm, the overlap can vary depending on the combinations of pattern dimensions, x and y. The pattern dimensions, (x, y), used in this study were (5.5, 1.5), (5, 2), (4.5, 2.5) and (4, 3).

The microstructure of SLS processed poly-Si film was investigated using SEM after Secco-etching. The width of poly-Si grains was measured by linear intercept method. Since the grain width varied depending on measurement position, the grain width was measured at positions of 1μm, 1.75μm, and 2.25μm away from the primary grain boundary. At each position, 3 measurements were done, and thus a total 9 measurements were done to calculate the average values of grain width for the individual specimens obtained in this study.

TFTs were fabricated on the SLS processed poly-Si film with various width of poly-Si grain. After SLS processing and poly-Si island patterning were done, 1000A-thick gate oxide was deposited by PECVD. MoW was sputtered as a gate metal and ion doping was used to form source and drain regions. The dimension of TFTs used in this work was 15μm in both channel width and length.

Ⅲ. RESULTS AND DISCUSSION

Fig. 2 shows the effects of overlap on the width of poly-Si grains. The pattern dimensions, (x, y), used in this study (See the notations in Section II and Fig. 1) were (4, 3) (Fig. 2 a) and (5, 2) (Fig. 2 b), resulting in the overlap of 0.5μm and 1.5μm, respectively. After 2-shot SLS process using the mask patterns, 3.5μm long poly-Si grains were obtained for both pattern dimensions (4,3) and (5,2), but the width of poly-Si grain made by pattern dimension (5, 2) was relatively larger than that made by pattern dimension (4, 3). The poly-Si grains crystallized after the 1st laser pulse became wide as the grains grow consuming the adjacent grains by competitive growth. By increasing the overlap between the 1st and the 2nd pulses, the zone re-molten by the 2nd laser pulse became in contact with a fewer number of previously crystallized grains which acted as seeds for the further lateral growth (Fig. 2b). As a result, the poly-Si grain width was increased by employing the mask pattern with large overlap.

Fig. 3 shows the poly-Si microstructures obtained by employing 2-shot SLS mask patterns. We could achieve poly-Si grains having various width but the fixed grain length, 3.5μm, by controlling the overlap between the 1st and the 2nd laser pulse without changing any process parameters such as film thickness of a-Si, laser pulse duration, laser fluence, and substrate temperature. The experimentally obtained data for grain width shows that as the overlap increased from 0.5μm to 2μm, the grain width increased by about three times compared to the grain width for the overlap of 0.5μm (Fig 4). The average grain widths for

the overlaps of 2μm, 1.5μm, 1μm and 0.5μm were 0.58±0.06μm, 0.51±0.09μm, 0.34±0.07μm, and 0.24±0.11μm, respectively.

For TFTs fabricated on SLS poly-Si film crystallized using 2μm-overlap mask pattern, we achieved the field effect mobility of 354±7.1cm^2/Vs for n-channel and 115±4.1cm^2/Vs for p-channel at V_{ds} = 0.1V (Fig. 5). The device threshold voltage was determined to be 1.18±0.19V for n-channel and –3.2±0.19V for p-channel TFT. A sharp turn-on with a sub-threshold slope of about 0.3V/decade was obtained for both n- and p-channel TFTs. The device had on-current of 3.5×10^{-5}A/μm (n-channel), 1.4×10^{-5}A/μm (p-channel) and off-current of 1.9×10^{-13}A/μm (n-channel), 7.1×10^{-15}A/μm (p-channel) when measured at V_{ds} = 5.1V.

Compared to 2μm overlap, 0.5μm overlap resulted in inferior TFT characteristics (Fig. 6). For example, the TFT field effect mobility for 0.5μm overlap was 269±26.7cm^2/Vs for n-channel, which was significantly lower than that for 2μm overlap (354±7.1cm^2/Vs). However, both 0.5μm and 2μm overlaps yielded similar p-channel mobility values of 112±10cm^2/Vs and 115±4.1cm^2/Vs, respectively. Our experimental results well agree with the research reported in the literature[1], which revealed that the p-channel TFT field effect mobility little depended on the poly-Si grain size when the grain size was larger than 0.3μm [1]. The threshold voltage of device was 1.67±0.87V for n-channel and –6.7±1.6V for p channel. The sub-threshold slope is about 0.5V/decade for both n- and p-channel TFT.

Fig. 7 shows the dependence of both field effect mobility and threshold voltage on the overlap between the 1st and the 2nd pulses as the overlap increased from 0.5μm to 2μm. When the overlap was 0.5μm, the field effect mobility was relatively low, ranging from 225cm^2/Vs to 302cm^2/Vs and the threshold voltage was relatively high, ranging from 1V to 4.2V. As the overlap increased from 0.5μm to 2μm, both field effect mobility and threshold voltage tended to be nearly constant with smaller variation (Fig. 7).) This is somewhat contrary to other results in the literature [4,7,14,21,22] which reported that for thin poly-Si films, as poly-Si grain width decreased, TFT field effect mobility tended to decrease. When the poly-Si grain width is larger than about 0.2μm, the n-channel TFT field effect mobility is little affected by the poly-Si grain width, however, the mobility is significantly decreased for the thinner film (Fig. 8). This is possibly because thin poly-Si film has high thermal stress during crystallization due to fast cooling rate compared to thick film, resulting in increase of intra-grain defects such as twin and sub-boundary[7,23-25], so that the film thickness may significantly affect TFT properties. On the contrary, the overlap variation little influences on the intra-grain defects in that the cooling rate during solidification is independent on the pattern dimension. Thus, one can expect nearly constant TFT properties although the overlap varies as shown in this study, in particular for the overlap greater than 0.5μm. This also indicates that TFT properties are not significantly affected by the grain boundaries parallel to the current flow from source to drain when the grain width is large enough to alleviate scattering of charge carriers due to the boundaries parallel to the current flow. However, the deterioration of TFT performance and uniformity for 0.5μm overlap seems to attribute to additional scattering centers. In this case, the grain width in the middle

of individual grains is so narrow that when TFT is on, the current should cross many grain boundaries included in TFT channel to flow from source to drain, which act as scattering centers for carrier transport[15,16].

Based on our results, we suggest a following design rule in making SLS mask pattern to achieve superior TFT properties and uniformities In 2-shot SLS process performed by employing mask pattern dimension, (x, y), as defined in Figure 1, the spacing of laser transparent slit on substrate, x, should be smaller than half of C-SLG (Controlled Super Lateral Growth) distance to avoid unwanted nucleation in the middle of laser transparent region [19,24].

$$x < 1/2 \text{ (C-SLG distance)} \quad (1)$$

Typically the C-SLG distance is known to depend on process parameters such as film thickness, laser fluence, pulse duration, spatial profile of laser pulse, and substrate conductivity [4,14,17] . Our results about TFT properties (Fig. 7) indicate that the overlap between 1st and 2nd laser pulse (*overlap* = $(x-y)/2$) should be not less than 1 μm.

$$(x-y)/2 \geq 1\mu m \quad (2)$$

Then, from equation (1) and (2), the spacing of transparent slit, x, should have values which fall in the following range;

$$2+y \leq x < 2\text{(C-SLG distance)} \quad (3)$$

Also the spacing of laser non-transparent region between two adjacent laser transparent slits, y, should be determined by optical resolution of projection lens used in SLS system, as

$$y > \text{(optical resolution)} \quad (4)$$

IV. CONCLUSIONS

Without changing other process parameters such as thickness of film, pulse duration, and laser fluence, we varied the width of poly-Si grain by employing the 2-shot SLS mask pattern for the variation of overlap between the 1st and the 2nd laser pulse. The poly-Si grain width decreased with decreasing the overlap. The measured TFT characteristics revealed that the width of poly-Si grain little influences on the device properties. We could achieve the TFT mobility about 350cm^2/V.sec for the overlap not less than 1μm. However, the TFTs fabricated with extremely narrow width of poly-Si grain have deterioration of TFT performances because many grain boundaries crossing the current flow direction included in the channel region of TFTs which act as a trapping sites for carrier transport. These results demonstrated that mask patterns should be designed that the overlap is not less than 1μm. The mask pattern (x, y) should be satisfied the condition that $2+y \leq x < 2$(***C-SLG distance***) and $y >$ (***optical resolution***) to achieve uniform TFT performances.

ACKNOWLEDGMENTS

The authors would like to thank members of Tech. Development Team 1 for their help in device fabrication and evaluation. We also acknowledge Prof. J.S. Im and Dr. A. Limanov at Coulumbia University for their helpful discussion on SLS technology. This work was financially supported by the Information Display R&D Center, one of the 21st Century Frontier R&D Program funded by the Ministry of Science and Technology of Korea.

REFERENCES

1. N. Ibaraki, SID '99 Digest, 172 (1999)

2. T. Nishibe, Eurodisplay, 2002, 269 (2002)

3. S.D. Brotherton, D.J. McCulloch, J.B. Clegg, and J.P. Gowers, IEEE Trans. Electron Device. 40, 407 (1993)

4. M. Hatano and T. Sjiba, SID 02 Digest, 158 (2002)

5. F. Takeuch, M. Takei, K. Hotta, K. Yoshino, K. Suga, A. Hara and N. Sasaki, , AM-LCD01, 251 (2001)

6. K. Yamazaki, T. Kudo, K. Seike, D. Ichishima, and C. Jin, AM-LCD02, 149 (2001)

7. A. Hara, F. Takeuchi, M. Takei, K. Suga, M. Chida, Y. Sano, and N. Sasaki, AMLCD'02, 227 (2002) 8. N. Sasaki, A. Hara, F. Takeuchi, Y. Mishima, T. Kakechi, K. Yoshino, and M. Takei, SID 2002 Digest, 154 (2002)

8. R.S. Sposili and J.S. Im, Appl. Phys. Lett. 69, 2864 (1996)

9. J.S. Im and R.S. Sposili, MRS Bulletin, 39 (1996)

10. J.S. Im, M.A. Crowder, R.S.Sposili, J.P.Leonard, H.J.Kim, J.H.Yoon, V.V.Gupta, H.J. Song, H.S. Cho, Phys. Stat. Sol. 166, 603 (1998)

11. J.Y. Park, H.H. Park, K.Y. Lee, H.D. Kim, H.K. Chung, AM-LCD03, 149 (2003)

12. M.A. Crowder, P.G. Carey, P.M. Smith, R.S. Sposili, H.S. Cho, J.S. Im, IEEE Electron Device Letters, 19, 306 (1998)

13. Y.H. Jung, J.M. Yoon, M.S. Yang, W.K. Park, H.S. Soh, MRS Symp. Proc., **621**, Q9.14.1 (2000)

14. S.D. Brotherton, M.A. Crowder, A.B. Limanov, B. Turk and J.S. Im, Asia Display/IDW'01, 387 (2001)

15. J. Y. W. Seto, J. Appl. Phys., **46**, 5247(1975)

16. T. I. Kamins, "Polycrystalline Silicon for Integrated Circuit Applications", (Kluwer Academic, Boston, 1988)

17. H.Takaoka, Y. Sato, T. Suzuki, T. Sasaki, h. Tanabe, H. Hayama, Asia Display/IDW '01, 395 (2001)

18. J.S. Im and H.J. Kim, Appl. Phys. Lett. 64, 2303 (1994)

19. H.J. Kim and J.S. Im, Appl. Phys. Lett. 68, 1513 (1996)

20. J.S. Im and H.J. Kim, Appl. Phys. Lett. 63, 1969 (1993)

21. P.S. Peercy, M. O. Thompson, and J.Y. Tsao, MRS Symp. Proc., 80, 39 (1987)

22. M. O. Thompson, G.J. Calvin, J.W. Mayer, P.S. Peercy, J. M. Poate, D. C. Jacobson, A.G. Cullis and N.G. Chew, Phys. Rev. Lett. 32, 2360, (1984)

23. M.A. Crowder, A.B. Limanov, and J.S. Im, Mater. Res. Soc. Symp. Proc. 621, Q 9.6 (2000)

24. H. S. Cho, D. Kim, A.B. Limanov, M.A. Crowder, and J.S. Im, Mater. Res. Soc. Symp. Proc. 621, Q 9.9 (2000)

25. K. kitahara, Y. Ohashi, R. Yamazaki, Y. Katoh, A. Hara and N. Sasaki, AM-LCD02, 53 (2003)

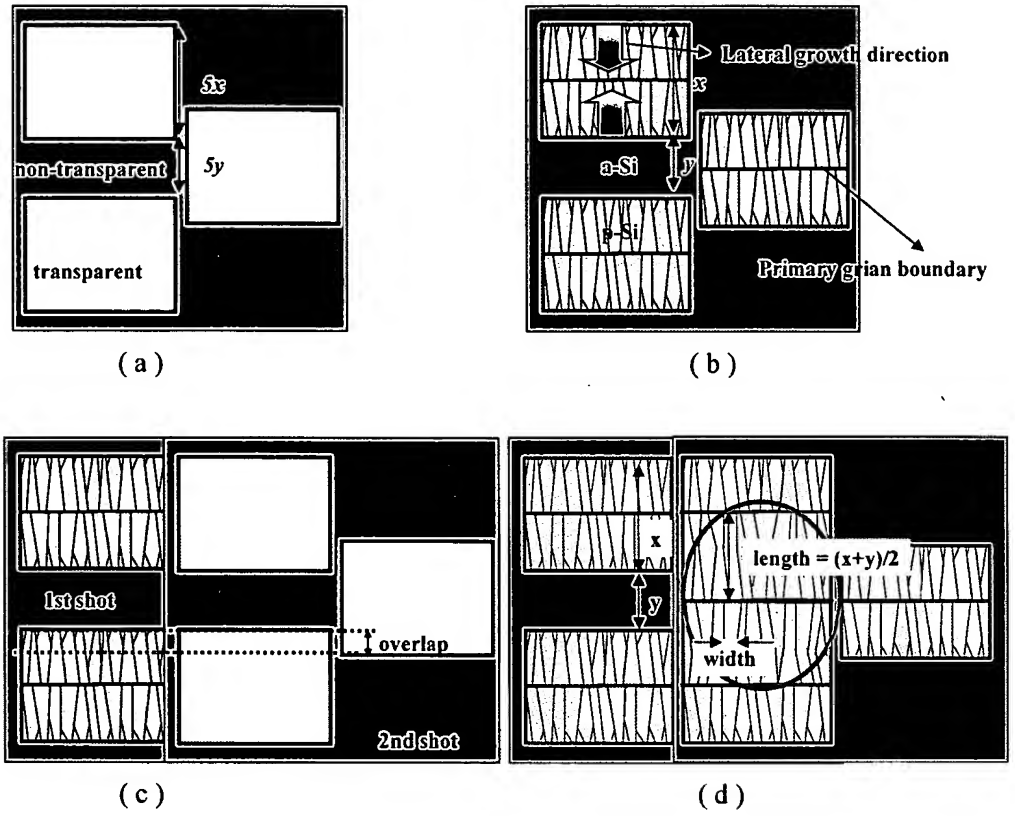
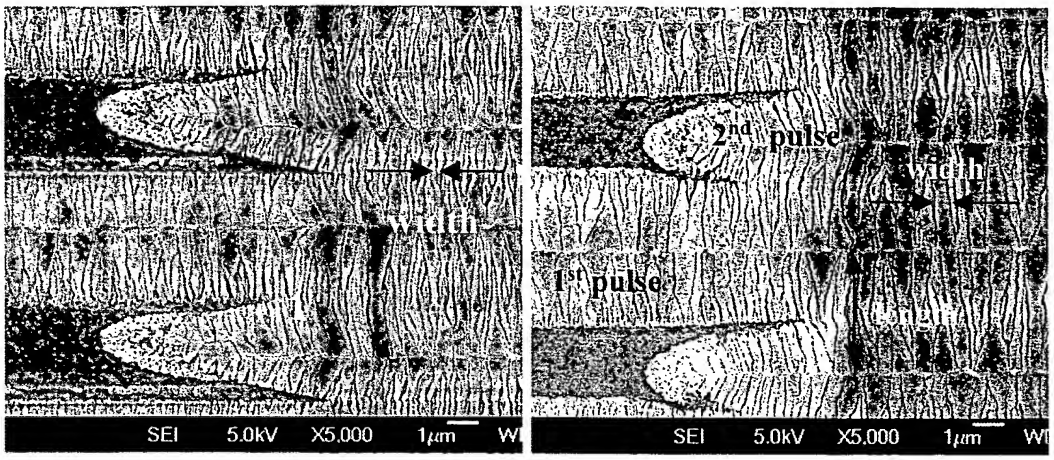


FIG. 1. Schematics illustrating 2 shot SLS process: (a) mask pattern, (b) grain structure after 1st shot irradiation, (c) translation of mask pattern, and (d) grain structure after 2nd shot irradiation.



(a) (b)

Fig. 2. SEM micrographs of Secco-etched 2-shot SLS processed poly-Si grains at the interface between the 1st and the 2nd laser pulses. The dimensions of mask pattern for microstructures (a) and (b) are (4, 3) and (5, 2), respectively.

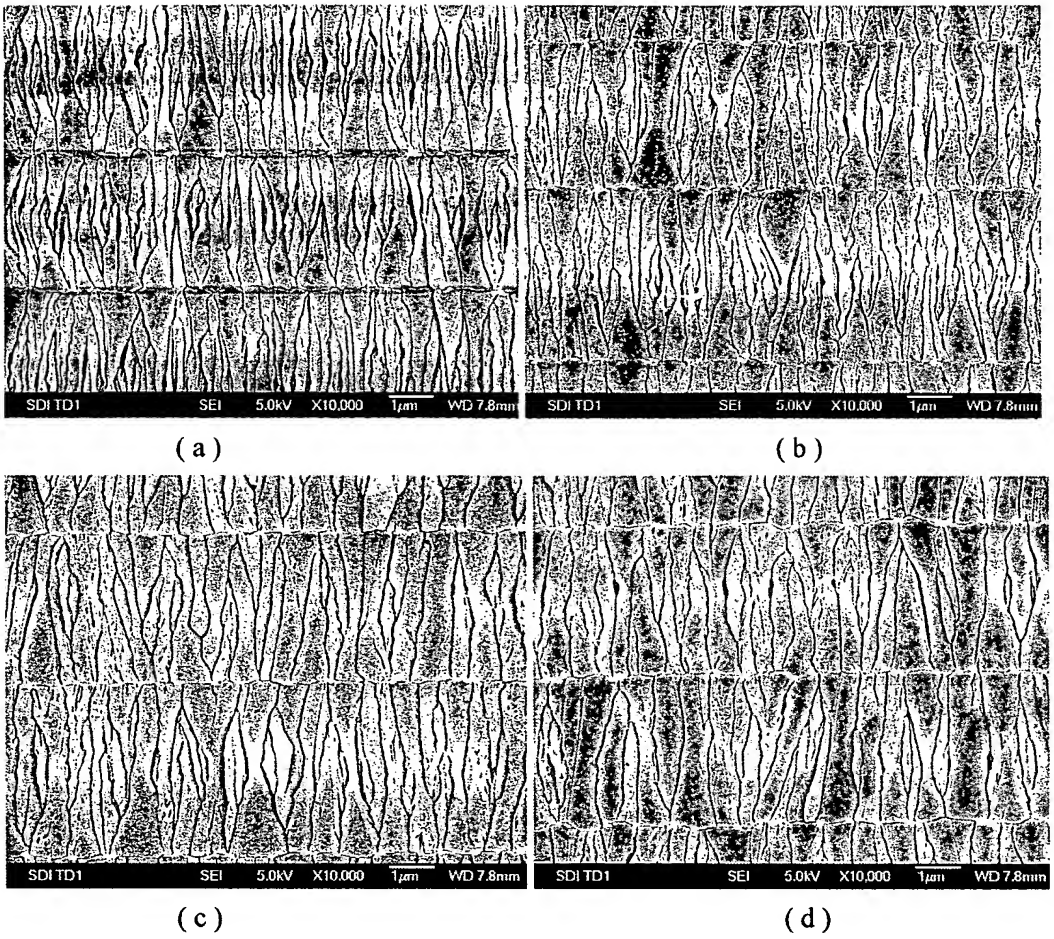


Fig. 3. SEM micrographs showing 2-shot SLS processed poly-Si microstructures obtained by employing different SLS mask pattern dimensions; (a) (4, 3), (b) (4.5, 2.5), (c) (5, 2), and (d) (5.5, 1.5). The corresponding overlaps were (a) 0.5μm, (b) 1μm, (c) 1.5μm, and (d) 2μm, respectively.

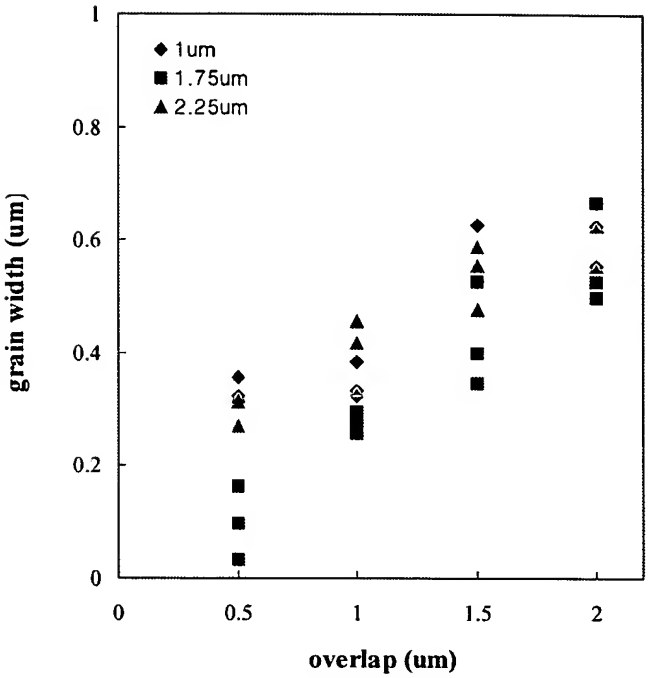


Fig. 4. Dependence of average grain width on the overlap between the 1st and the 2nd laser pulses. The grain width was measured at positions of 1μm, 1.75μm, and 2.25μm away from the primary grain boundary.

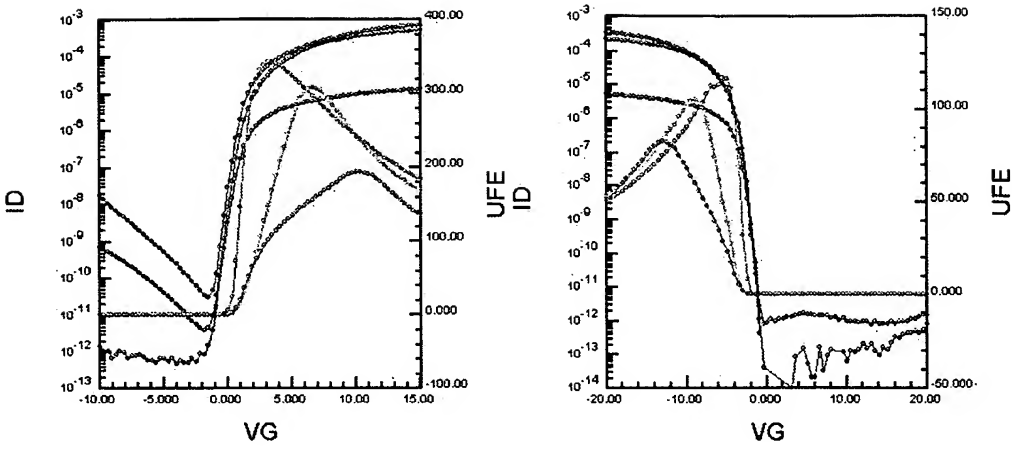
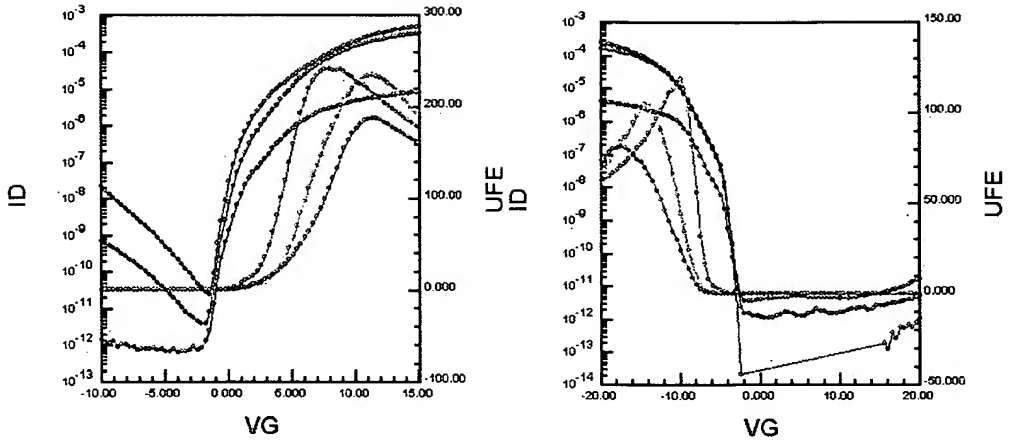
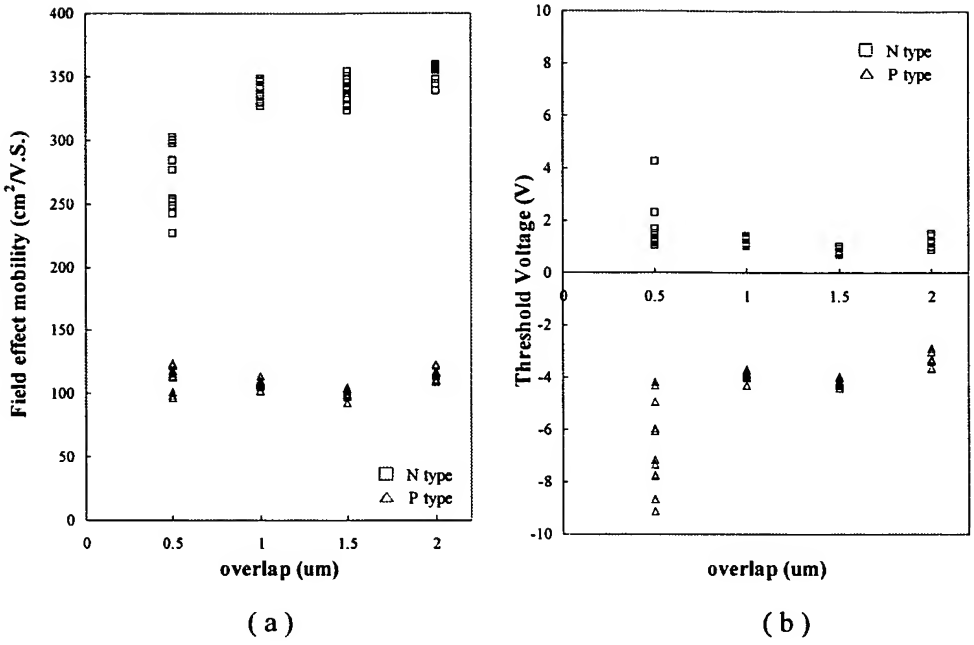


Fig. 5 I_d-V_G characteristics and TFT field effect mobility for the poly-Si film crystallized with (5.5, 1.5) mask pattern; (a) n-channel and (b) p-channel. The channel dimension was 15μm in both channel width and length. TFT parameters were measured at V_{ds} = 0.1V, 5.1V, and 10.1V.



(a) (b)

Fig. 6 I_d-V_G characteristics and field effect mobility of poly-Si film crystallized with (4, 3) mask pattern. (a) n-channel and (b) p-channel TFT with 15μm in both channel width and length. V_{ds} = 0.1V, 5.1V, 10.1V



(a) (b)

Fig. 7. Dependence of (a) field effect mobility and (b) threshold voltage on the overlap between the 1st and the 2nd laser pulses.

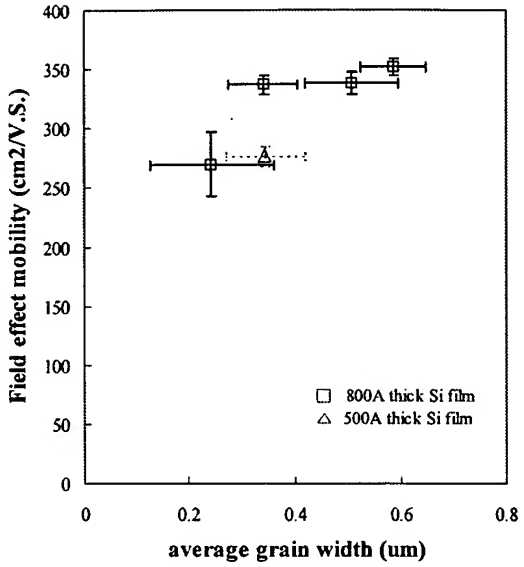


Fig. 8. Dependence of n-channel TFT field effect mobility on the poly-Si grain width. The Si film thickness is 800A and 500A. The overlap between the 1st and the 2nd laser pulse are 0.5μm, 1μm, 1.5μm, and 2μm, respectively for 800A thick Si film and 2μm for 500A thick Si film.